

Product Description

The IP00C814 is an enhanced multi-functional image processing LSI with integrated 2-channel scalers and de-interlace cores as well as a 1-channel warping engine. It can accept 4K dual input images with 2K PiP/PoP output images and single 4K input image with 4K output image. This device has an embedded CPU, and peripherals such as JPEG codec, HDMI Rx, high-speed ADC, video decoder, and LVDS/V-by-One®HS Tx. In addition, high-performance functions such as HDR, 3DLUT for color management and edge-blending required for multi-screen system with multiple projectors are also integrated.

Features

Input (2-port)

- RGB 30bit / YUV 4:4:4 30bit / YUV 4:2:2 20bit / YUV 4:2:2 10bit / YUV 4:2:0 30bit
- HDMI (2-port) / LV-CMOS (2-port) / Analog RGB / CVBS

Output (2-port)

- RGB 30bit / YUV 4:4:4 30bit / YUV 4:2:2 20bit / YUV 4:2:2 10bit / YUV 4:2:0 30bit
- Dual LVDS (2-port) / V-by-One®HS

Input & Output Image Size

- Horizontal sync signal 16,384 pixels
- Horizontal image active area 2,176 pixels

External DDR3-SDRAM

- Scaler frame memory : 32bit PC1600 (4G/2G/1G×16) ×2
- Arm® main memory : 16bit PC1600 (4G/2G/1G×16) ×1

External / Internal Sync

- Output sync signal is available only with internal sync signal

Input / Output Sync / Asynchronous Behavior

- Frame rate conversion with frame tear protection
- External force synchronization • Genlock

HDMI Rx

- Compliant with HDMI 2.0b and HDCP2.3 (support DV11.0)
- Embedded HDCP Key
- Audio interface supports L-PCM and Compressed audio data

High-speed ADC

- Maximum operating frequency 165Mhz
- Hsync/Vsync separate input supported
- Clock phase adjustment 32steps • Sync on Green input supported

Video Decoder

- NTSC-M, JPN, 4.43 / PAL-B, D, G, H, I, N, M, CombinationN, 60 / SECAM
- VBI (Closed Caption / CGMS / WSS) data extraction
- Clamp pulse output

Embedded CPU

- Arm Cortex®-A9 (660MHz)
- Cache L1 : 32KB Instruction 32KB Data L2 : 128KB
- Boot Serial flash/eMMC/EEPROM(I2C Ch4) selectable
- Work RAM 128KB
- 8-bit parallel / 4-wire serial when external CPU is in use

CPU peripherals

- Ethernet(10/100/1000Mbps), USB2.0 (Host/Device 2ch), SD Card, eMMC • JPEG Codec
- DMA (8ch) / UART (5ch) / I2C (4ch) / Timer (4ch) / IR remote control (3ch) / 10bit ADC (8ch, MUX) / 10bit DAC (3ch)

4K Dual Input PiP De-interlacer/ Scaler/Warping LSI



External Interface

- External interrupt (4ch) • Serial flash interface

Motion Adaptive De-interlacer

- YUV4:2:2 • All major cadences supported
- Motion adaptive filter based on Y,U,V

Scaler

- Zoom/shrink 6-symbol programmable FIR filter (10bit/pixel)
- Embedded coefficient ROM (64sets)

Distortion Correction

- RGB independent distortion correction
- Coordinate correction look up table
- Embedded warp table generator (keystone correction and pin cushion correction)
- Load from external CPU or external serial flash
- Up to 45 degrees (horizontal / vertical)

Noise Reduction

- 3DNR (H, V, Temporal) • MPEG-NR (Mosquito, Block)
- Chroma error filter

Image Correction

- Edge-blending (RGB independent gamma correction, white peaking supported)
- Mirror / flip image, 90 degree rotation
- Overlay, Alpha blending, Color key blending

Image Quality Control

- 3DLUT
- Static HDR (PQ, HLG), Dynamic HDR (SMTPE2094-10,40)
- H/V edge enhancement (9 symbols)
- 16-bit color gamma correction tables (7 LUT available)
- Error diffusion, brightness and contrast adjustment

Bitmap OSD

- 256 colors / High color OSD (64K colors)
- Embedded font engine (65536 words)
- Blinking and semi-transparent (4 colors OSD)
- 90-degree rotation, OSD scroll
- Bitmap transfer from external serial flash

Power Supply

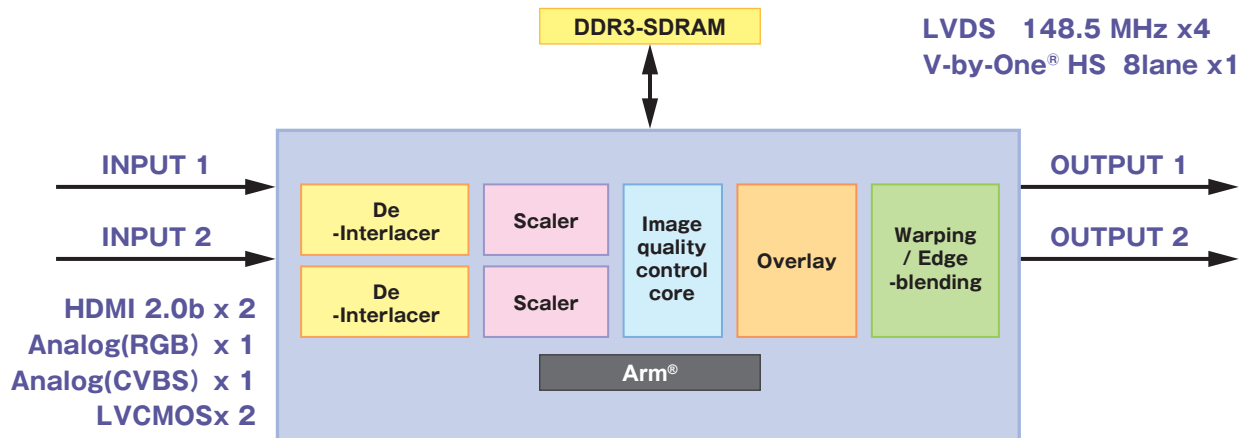
- 3.3V / 2.5V / 1.5V / 1.2V / 1.1V

Package

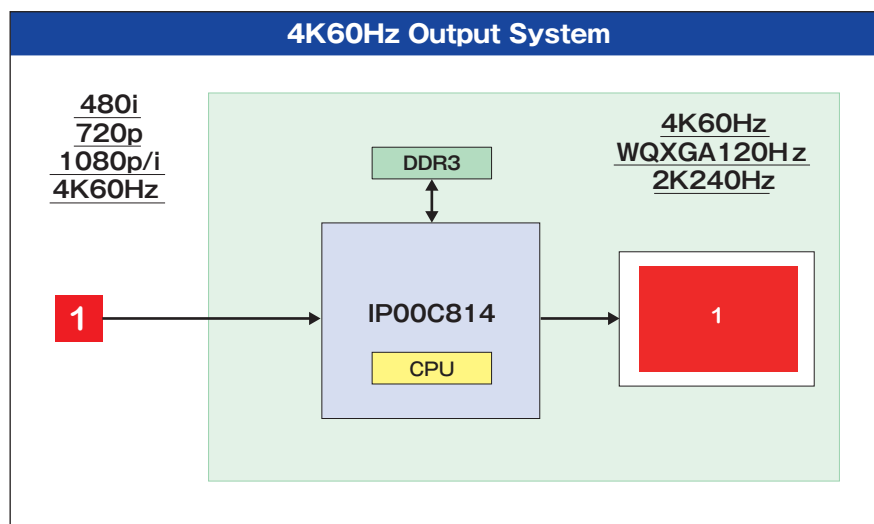
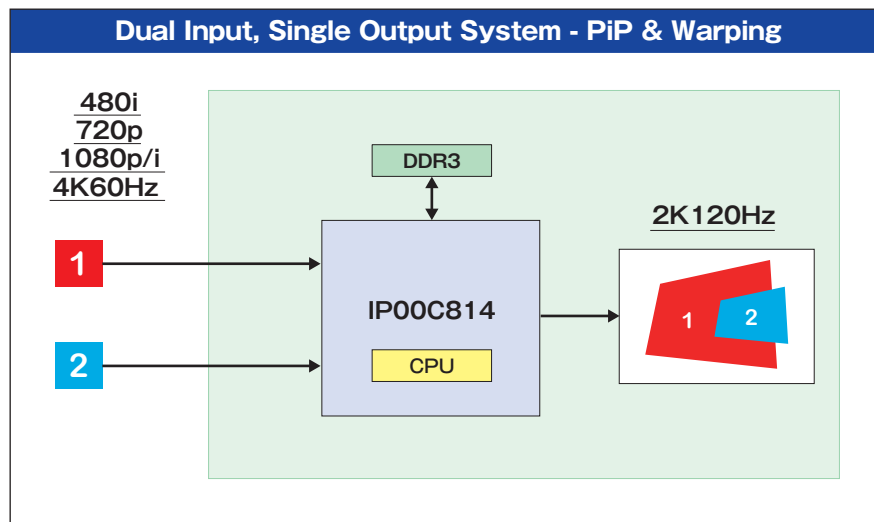
- 840-pin Plastic BGA (0.8mm pitch), 31mm x 31mm

IP00C814 4K Dual Input PiP De-interlacer/Scaler/Warping LSI

Block Diagram



Application Diagrams



"V-by-One®" is trademark of THine Electronics, Inc.
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